DIGITAL ELECTRONICS

REFERENCES

Theory:

L.R. Fortney, *Principles of Electronics*, chapter 9
F.J. Holler, J.P. Avery, S.R. Crouch, and C.G. Enke,
Experiments in Electronics, Instrumentation and Microcomputers
Don Lancaster, *TTL Cookbook*

Electrical instruments and Circuit wiring:

Chapter "Circuit Wiring Technique" in the Lab Manual
Chapter "Commonly Used Instruments" on *The Oscilloscope* and *The Multimeter* in the Lab Manual

I
INTRODUCTION

This experiment is a basic introduction to digital logic. You should attempt it only if you either have some prior facility with circuit wiring **or** you have completed one of the electrical experiments (e.g., DC Circuits I, Charge and Discharge of a Capacitor).

The experiment investigates how transistor devices are used to make various logic circuits. It is in two parts, each part having a value of one weight. Part I studies the Basic Unit, AND gates, OR gates, and binary adders. Part II studies Bistables, flip-flops, memories, and timing devices. All these components are available at the **R**esource **C**entre. The experiments do not investigate WHY a transistor behaves as it does, but concentrates on WHAT it does. As the circuits studied become progressively more complex, the experiments tend more towards logic than electronics.

The modules stack together, and are powered by 5 Volts DC from the power supply. The modules refer to a 6 V supply, but they work well at 5 Volts. This guide sheet, in addition to being divided into two parts, has a number of sections. When finished one section, turn off the power and remove all wires before going on to the next.

PART I

I.1 - THE BASIC UNIT

The Basic Unit is the simplest "blackbox" (actually grey) in the experiment. It contains a single n-p-n transistor, with three parallel inputs and two outputs. The circuit diagram is shown in Figure 1. Turn over the Basic Unit and identify the components. The "b", "c" and "e" stand for the base, collector and emitter of the transistor, and since the emitter is connected to the 0 Volt reference level for both the input and output, this circuit is called a common emitter configuration.

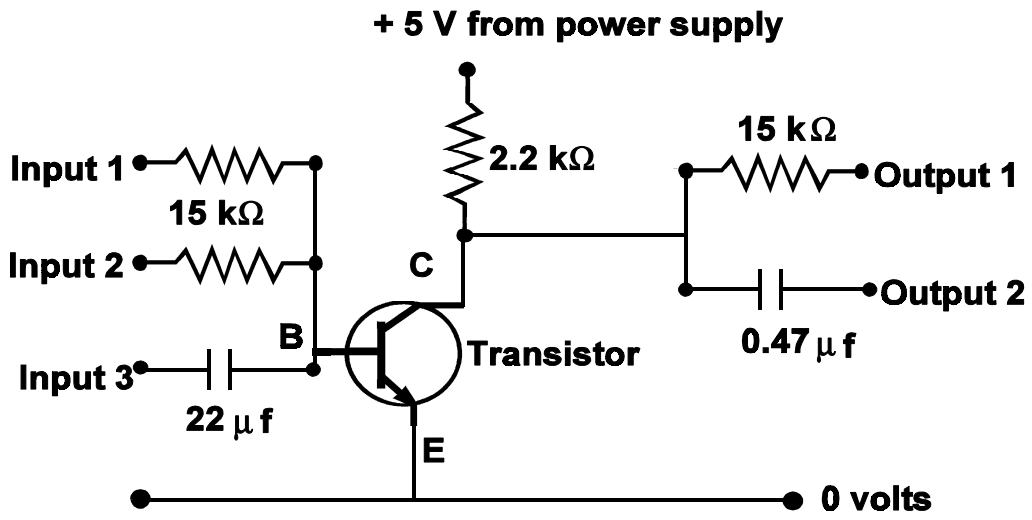


Figure 1.- Circuit of the Basic Unit

In this section we investigate output voltage *versus* input voltage. Rather than using a second power supply for the input voltage, we use a potentiometer as in Figure 2a. Wire up the potentiometer circuit and use a voltmeter to investigate how it produces a variable voltage.

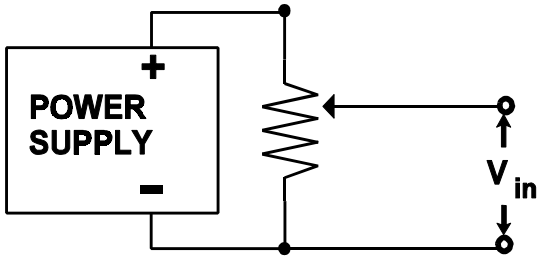


Figure 2a.

Figure 2b shows the circuit which can be used to show the amplifying properties of the transistor. Note that in this figure we have not detailed the power supply. In electronic circuit diagrams the power supply is usually not shown, and we will continue this convention; you may assume that it is always there, however!

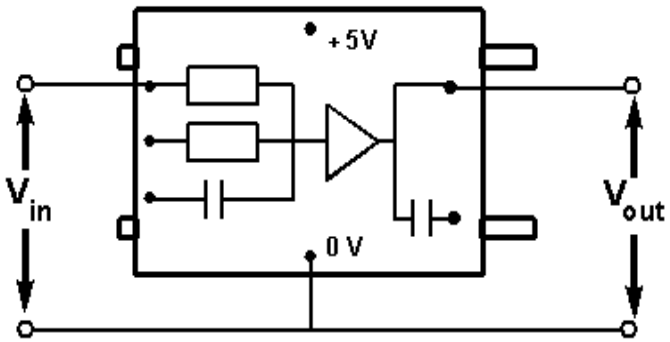


Figure 2b.

Wire the power supply to the left side of the Basic Unit, red-to-red and black-to-black, then turn the system on. It is a good idea to keep the power supply on while you are wiring up your circuits. This way you can monitor any short circuits that you may encounter. You may measure V_{out} for various V_{in} by changing the potentiometer, paying particular attention to the range where V_{out} changes most rapidly.

When the potentiometer is set so V_{out} is 3.0 Volts, small changes in V_{in} give large changes in V_{out}. Thus, when the transistor is "biased" with the potentiometer, it may be used as an amplifier.

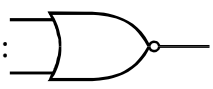
What would the gain ($= \Delta V_{out} / \Delta V_{in}$) be for your Basic Unit?

Why do most non-inverting transistor amplifiers have an even (2,4,6, ...) number of transistors?

If high voltage (5.0 Volts) is assigned the value 1, low volts the value 0, then the action of the Basic Unit can be summarized in the following Truth Table:

INPUT 1	INPUT 2	OUTPUT 1
0	0	1
1	0	0
0	1	0
1	1	0

Verify this table for your Basic Unit. In logic circuits, this truth table defines a

NOR gate, symbolized as: 

(Incidentally, the symbol on the Basic Unit stands for amplifier.) 

Before proceeding to further sections, turn off the power and remove all wires and the potentiometer from the Basic Unit so you may make a fresh start on Section 2.

I.2 - "AND" GATES

Set up the circuit shown in Figure 3 using three Basic Units. Inputs 1 and 2 can be just wires connected as shown. to make an input high, just plug into any of the sockets marked +6V; to make an input low, plug into any socket marked 0V. Your may turn the boxes over to verify that any +6V socket is equivalent.
The indicator lights-up when the input is high, goes out when the input is low. Examine the circuit of the Indicator and explain how it works. Thus the Indicator shows whether the output of the circuit is high or low. (Most of our Indicators have 3 separate lights in one box.)

Can you *predict* the truth table for this configuration? The logic diagram for these three NOR gates set up like this may help you. Now, measure the truth table for your circuit. In logic circuits, this device is called an AND gate,

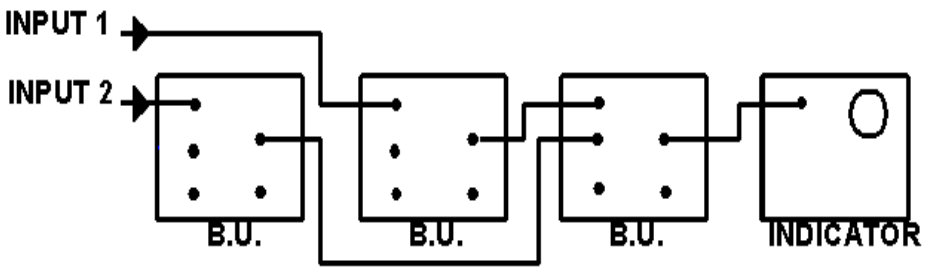
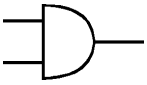


Figure 3.

and is symbolized by : 

In fact, one of the supplied modules is an AND gate. Verify that the ready-made AND gate has the same logic as the one you have constructed. Then, turn the AND gate over and trace out its circuit to see why.

I.3 - BINARY ADDITION

The truth table for addition of two one digit binary numbers is:

INPUT 1	INPUT 2	CARRY	SUM
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

The logic diagram for such a circuit is shown in Figure 4.

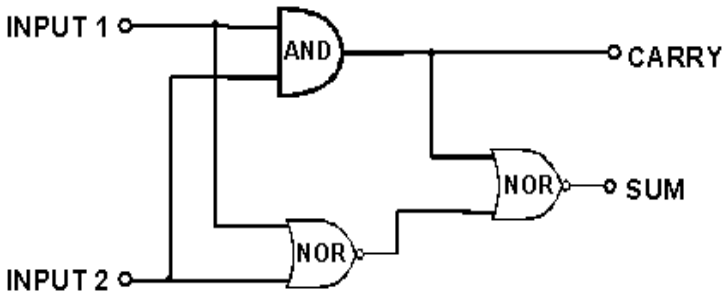


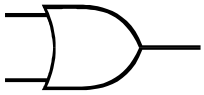
Figure 4. - Binary Addition

Verify that this does satisfy the above truth table, and then build it using two Basic Units and an AND gate to prove that it works. This circuit is called a Half Adder.

I.4 - "OR" GATE

This time we only supply the truth table, and challenge you to build the corresponding OR gate. Check your logic by testing your circuit.

INPUT 1	INPUT 2	OUTPUT 1
0	0	0
1	0	1
0	1	1
1	1	1

The symbol for an OR gate is: 

Note it is similar but not identical to the symbol for a NOR gate.

I.5 - FULL ADDERS

This section discusses full binary addition, and contains no experiment.

The adder of Section 3 can take two binary digits and add them. But when adding numbers with more than one bit, provision has to be made for the carry bit too. Such a Full Adder uses two Half Adders as in Section 3 plus an OR gate, as shown in Figure 5.
Write out the truth table for the Full Adder.

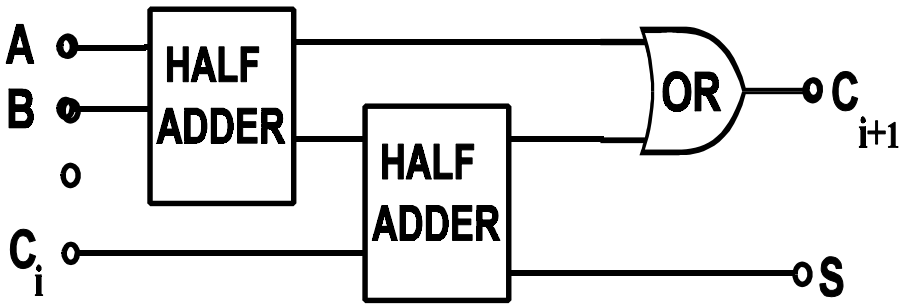


Figure 5. - Full Adder

Addition of two 3-digit binary numbers, A and B, can thus be accomplished as shown in Figure 6.

Just as the AND Gate combined 3 transistors as NOR gates in one box, this circuit could be put in one box too, but the number of transistors is large. (How many?) However, an Integrated Circuit can be `grown' with this circuitry and end up no larger than the head of a match.

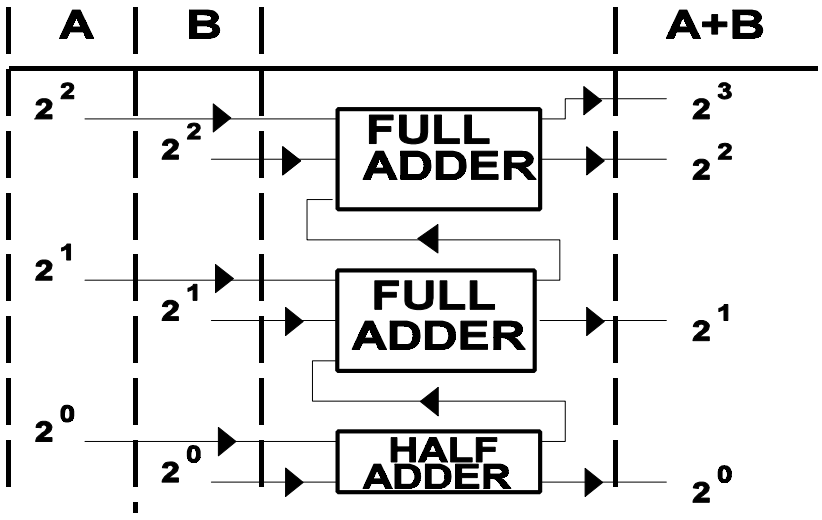


Figure 6.

PART II

INTRODUCTION

This is a continuation of Part I. Here you investigate more advanced logic circuits.

In Part I the circuits you studied were built up from combinations of simple n-p-n transistors. Most of your work in Part II will be using integrated circuits ("chips") from the family of Transistor-Transistor-Logic (TTL) components.

You will find that whereas the Guide Sheet for Part I tended to be more-or-less explicit as to what to do, Part II is intended much more as an introduction that will get you thinking about what you want to do. You will find the references useful in exploring the question of what you wish to learn from this experiment.

> **TTL circuits must never be driven by more than 5.0 Volts DC, and will not work properly at less than 4.7 volts DC.**

II.1 - THE TTL "NOR" GATE

Find the module labelled "7402". This box contains an integrated circuit containing four NOR gates. The numbered jacks on the top of the box are wired to the pins on the "chip" in accordance with Figure 7.

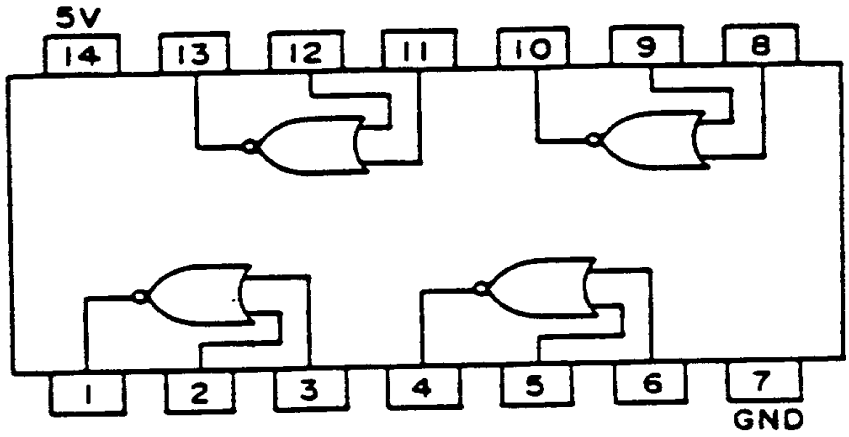


Figure 7. - Pin Assignments of 7402 Circuit

Note that three pins are used for each NOR gate in the chip. Also, pin 14 is the +5V power lead for the circuit, and is also connected to the positive input for the power supply on the side of the box. Similarly, pin 7 is the 0V ground lead and is connected to the other power supply input on the side of the box.

Verify that the logic of the 7402 NOR gate is identical to the Basic Unit using one of the gates in the module.

- In Part I you probably assumed (correctly) that any input not connected to anything would be low. This is not correct for TTL circuits. An unconnected input is unpredictable for TTL gates (though the tendency is that unconnected inputs swing "high". **Thus all inputs (used or unused) for these circuits must be explicitly wired to be either high (5.0 Volts) or low (0 volts).**

The circuit for the NOR gate of the 7402 chip is not the simple transistor of the Basic Unit. For those interested, we recommend looking at the Appendix at the end of this Guide Sheet which discusses the TTL circuit. In any case, one reason why TTL is preferred to a simple transistor is related to the speed of response.

You may compare the speed of the TTL NOR gate to the Basic Unit as follows.

- Using the oscilloscope in DC mode, set the signal generator so that it is delivering a 100 kHz square wave with a DC offset so that the voltage varies between 0 Volts and +5.0 volts. Do not connect the NOR gate until you have made this adjustment. If you are unsure how to use the oscilloscope, please refer to the “Commonly Used Instruments” section on the “Oscilloscope” of the **Laboratory Manual .**
- Keep the output of the generator wired to the oscilloscope, and also wire the output in parallel to one of the inputs of the NOR gate to be tested. Wire the output of the gate to the other beam of the oscilloscope.

You may now measure the speed of response of the NOR gate to changing inputs.

II.2 - "NAND" GATES

The NAND gate has the same logical relationship to the AND gate that the NOR gate has to the OR gate. Can you therefore predict the truth table for a NAND gate?

The module labelled “7400’’ contains four NAND gates with pin assignments as shown in Figure 8. Use one of the NAND's in the 7400 to check your prediction of the truth table.

For reasons explained in the Appendix, the NAND gate is the "Basic Unit" of TTL circuits, and thus has the lowest number in the 7400 series of integrated circuits.
QUESTION: A seat belt warning system is to sound a warning buzzer unless all passengers have their seat belts fastened. The warning buzzer is to sound unless the driver's belt is fastened and each of the other seat belts are fastened or there is no weight on the seat. Assume there are "high" true logic signals representing the following: SS = start switch on; SB1 = driver seat belt fastened; SB2, SB3, SB4 = other belts fastened; W2, W3, W4 = weight sensed on seats 2, 3 and 4. Using 7400 and 7402 TTL chips, how can this be implemented? You will probably find that using the 7400 and 7402 modules to design, for example, an AND gate and then using the AND gate in your logic will be useful.

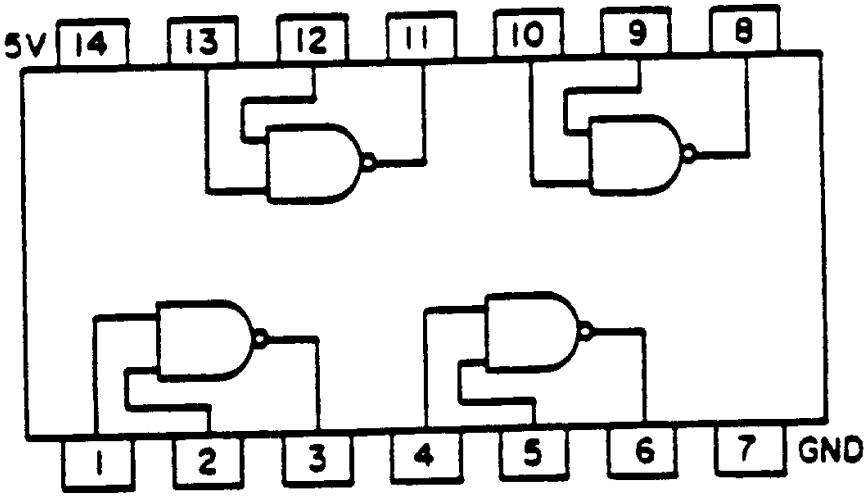


Figure 8. - Pin Assignments of 7400 NAND

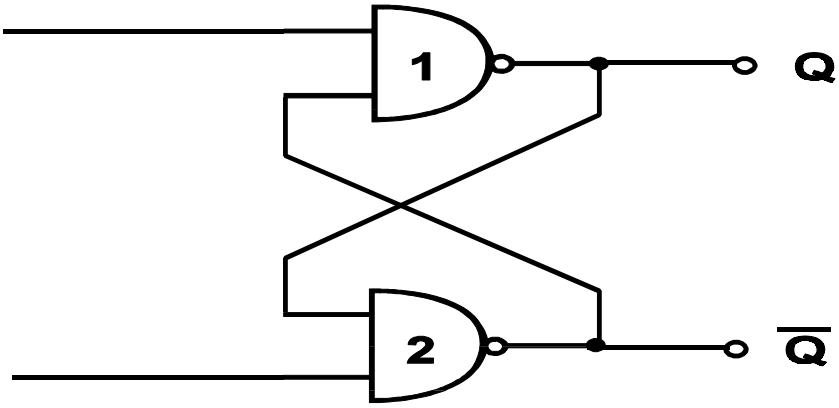


Fig 9. - NAND gates used to build a latch

II.3 - LATCHES AND FLIP-FLOPS

Using two of the NAND gates in the 7400 module, wire the latch circuit shown in Figure 9.

Connect the outputs Q and $\overline{Q}$ to indicators, and the inputs S and R to switches. (S and R stand for Set and Reset; the nomenclature Q and $\overline{Q}$ should be clear to you after you have investigated the circuit.)

Hold down both switches simultaneously, so the inputs are High. Then momentarily release the switch connected to the gate whose output is Low and observe the result. Why is this circuit called a latch? Why are the two outputs labelled Q and $\overline{Q}$? Can you follow the logic and explain why this circuit behaves as it does? Now use the other two NAND gates in the 7400 chip to modify your latch into the "S-R clocked flip-flop" shown in Figure 10.

The inputs S and R can be wires which you will connect to either High or Low voltage sources; the "Ck" input should be connected to the Switch module. Set the inputs S and R so they are opposite, leave the switch so the Ck input is Low, and power the circuit up. Observe what happens when the Switch is momentarily pressed and released. What happens when the Switch is pressed again? If you reverse the S and R inputs what happens? What happens when the switch is pressed and released?

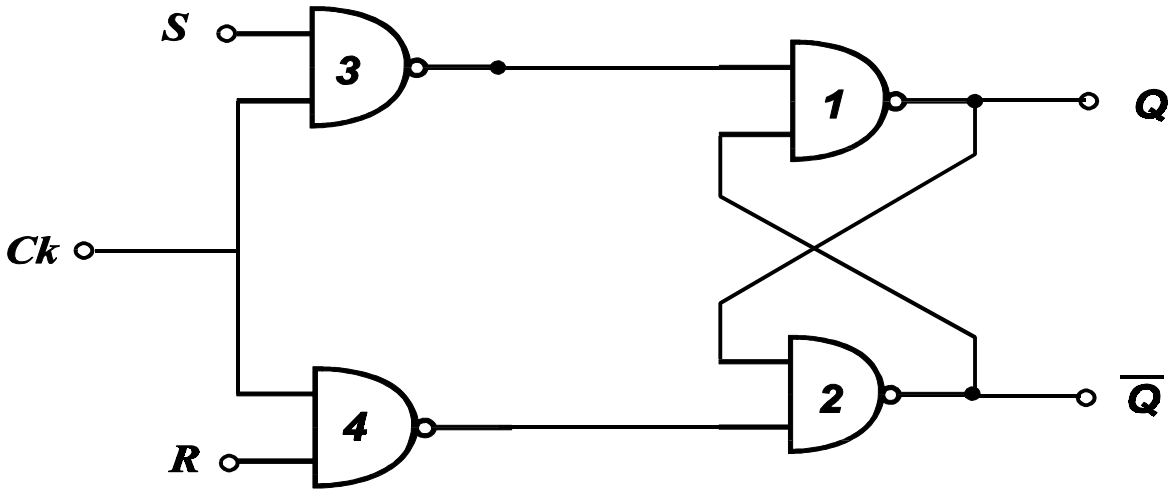


Figure 10. - S-R clocked flip-flop

Thus, the S-R clocked flip flop acts as a one-bit memory circuit that allows, for example, the Q output to match the S input on the application of a positive level at Ck. The Ck stands for clock; in a computer, for example, the internal clock determines the cycle time for the memory.

The Truth Table for the S-R clocked flip-flop is shown below.

S_n	R_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	?

Verify the validity of this truth table, and investigate the meaning of the "?" in the final row. Note that the subscripts *n* and *n* + 1 refer to the state after clock pulses *n* and *n* + 1 respectively.

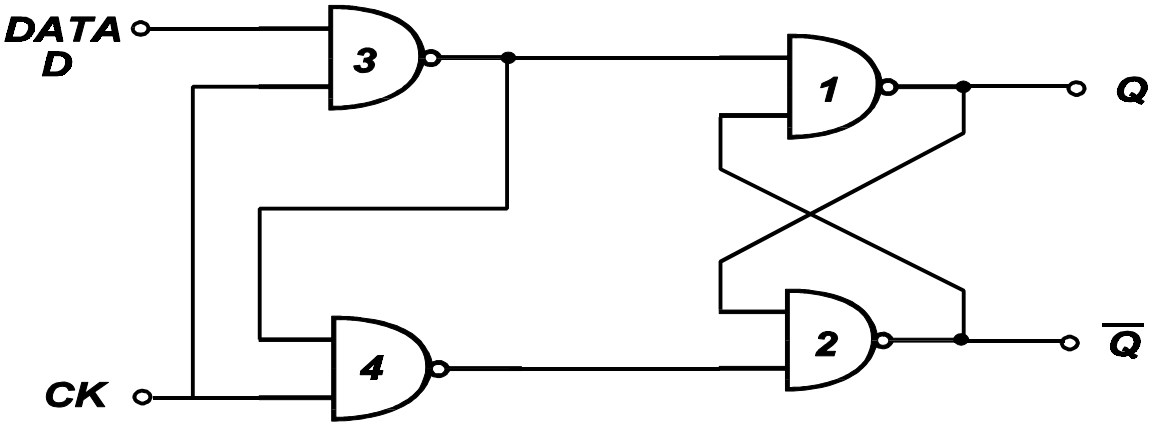


Figure 11.- D(delay) flip-flop

Now modify your flip-flop circuit into the D (Delay) flip-flop shown in Figure 11. Investigate its truth table, and determine why this is called a delay flip-flop. Compare its logic to the 7474 circuit whose pin assignments are shown in Figure 12.

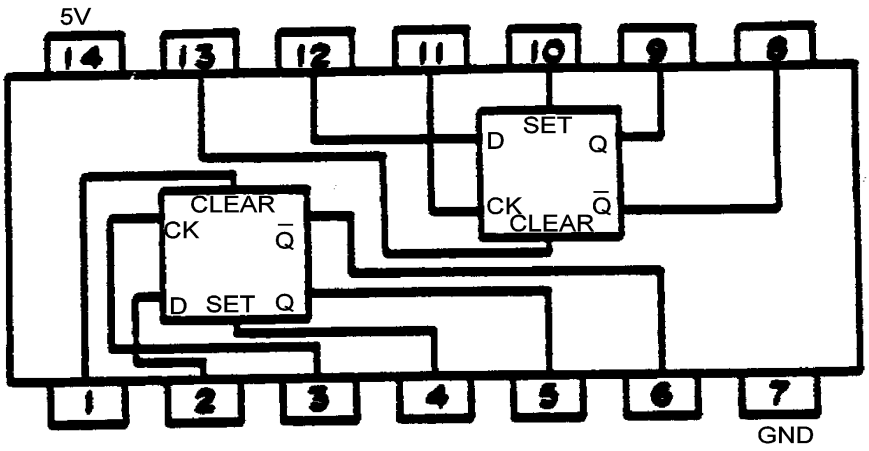


Figure 12. - 7474 Dual D flip-flop

II.4 - OTHER POSSIBILITIES

We have supplied you in module form two more TTL chips which in conjunction with various references can take you fairly far along your investigation of digital electronics. The pin assignments are shown in Figures 13, 14. For the really keen, after consultation with your demonstrator we can arrange to make available virtually the entire line of TTL chips in breadboard form.

Also, in the "store-bought" modules are two non-integrated circuits, the Multivibrator and Bistable, which you may investigate.

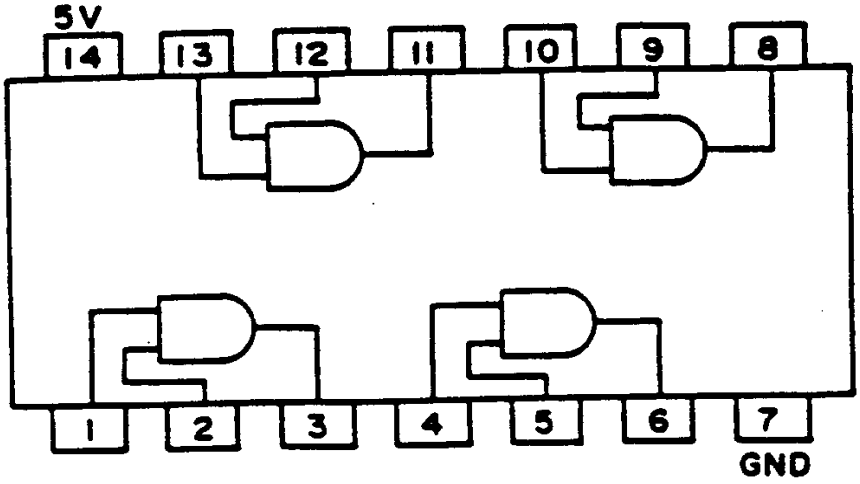


Figure 13. - 7408 Quad AND

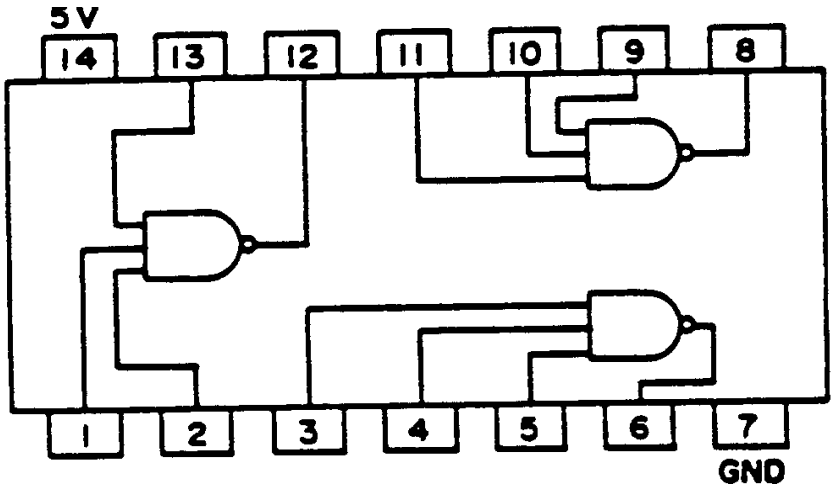


Figure 14.- 7410 3-input NAND

APPENDIX

In the "store-bought" circuits studied in Part I, the basic circuit was the NOR gate, implemented by a single n-p-n transistor. All other logic functions were built up from this basic logic function.

The basic circuit of the TTL systems studied in this experiment is the NAND gate, and other logic functions are built up from combinations of this gate. The logic of the NAND gate is studied in Section 2 of this Guide Sheet. Can you see, for example, how to build a NOR gate from NAND gates?

The circuit of the TTL NAND gate is shown if Figure 15.

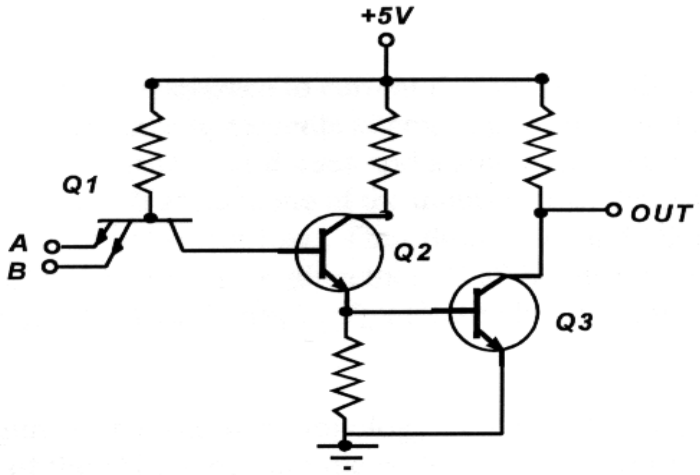


Figure 15. - A TTL NAND gate

Q1 is a multiple-emitter transistor which is easily and cheaply built with modern integrated circuit technologies.

In order to understand how this circuit works, look at Figure 16.

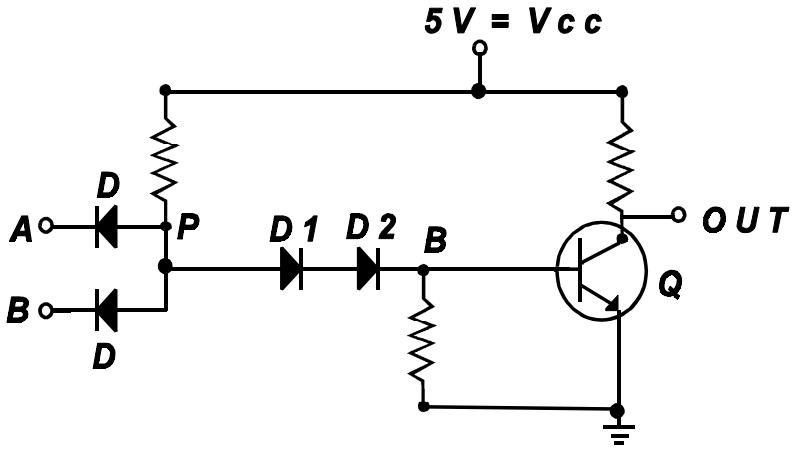


Figure 16. - A DTL NAND gate

The symbol stands for a diode. 

A diode presents essentially no resistance to current flowing in the direction of the "arrowhead", but gives essentially infinite resistance to currents attempting to flow in the opposite direction. Figure 16 shows a NAND gate constructed of diodes and a single transistor; such gates are called Diode Transistor Logic (DTL) gates. If at least one of the inputs is low, the diode D connected to this input conducts, and the voltage at point P is low. Thus diodes D1 and D2 are non conducting, and the input to the transistor Q is low, giving a high output. If all inputs are high, then all input diodes are cut off. Then the voltage at P tries to rise to V_{cc} effectively giving the transistor a high input at B, giving a low output.

The TTL circuit of figure 15 has the same topology as Figure 16. The emitter junctions of Q1 act as the input diodes D of the DTL gate, and the collect of junction of Q1 replaces the diode D1 of Figure 16. The base-to-emitter diode of Q2 is used in place of the diode D2 of the DTL gate, and both circuits have an output transistor (Q3 or Q).

Clamping diodes are often but not always included in the TTL NAND gate from each input to ground, with the anode grounded. These diodes are effectively out of the circuit for positive input signals, but for negative voltage excursions they limit the input to a safe value.

(dh - 1982, jbv - 1990)